Journal of NUCLEAR SCIENCE and TECHNOLOGY, Supplement 4, p. 279–282 (March 2004)

Development of a High Resolution APD Based Animal PET and Multi-Channel Waveform Sampling Front-End ASIC

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A new Waveform Sampling Front-End (WSFE) Application Specific Integrated Circuit (ASIC) for Positron Emission Tomography (PET) has been developed to digitize signals from scintillating crystals at an early stage. Each channel of the chip consists of a preamplifier, a variable gain amplifier (VGA) and a fast Analog to Digital Converter (ADC). This aggressive approach to signal processing has several advantages over conventional method such as suppression of noise and flexibility in choice of signal processing methods while allowing many channels to be readout individually due to its low power consumption. Two such chips have been designed and experimental results are presented in this paper.

I. Introduction

As the spatial resolution of next generation Positron Emission Tomography (PET) cameras are being pushed to their limits, given a specific geometry, the only way to improve the resolution is to reduce the intrinsic resolution of the detector module. This implies using smaller scintillating crystals which will greatly increase the number of channels. Thus, the use of Application Specific Integrated Circuits (ASIC) as the front-end electronics seems appropriate given their miniscule size and much lower power consumption compared to conventional discrete analog electronics.

A next generation Avalanche Photodiode (APD) based animal PET has been proposed and a Waveform Sampling Front-End (WSFE) ASIC has been developed. Each small scintillating crystal is coupled to a pixel of a multi-array APD[1)] and the signal will be digitized by the WSFE ASIC at an early stage.

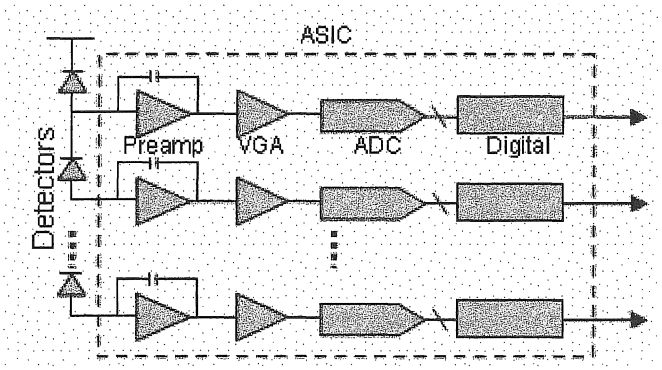

Fig. 1 Layout of the WSFE ASIC

Two WSFE ASICs has been designed using Rohm 0.35 μ CMOS ASIC technology. Each channel of the WSFE consists of a preamplifier, a VGA and a fast ADC (see **fig. 1**). The preamplifier picks up detector signals and feeds them to the VGA which adjusts the amplitude to the maximum input range of the ADC. The ADC samples the amplified output signals of the VGA and converts them into digital waveforms to be temporarily stored by the FIFO buffer. Such a scheme not only simplifies the electronics and improves the signal to noise ratio, it also allows complex signal processing such as pulse shape discrimination (PSD) to be carried out to obtain depth-of-interaction (DOI) information when crystals of different decay times are stacked as in **Fig. 2** [2)]. Since APDs are almost transparent to annihilation gamma rays, a multi-layered module can be implemented to improve the efficiency and provide even finer DOI information.

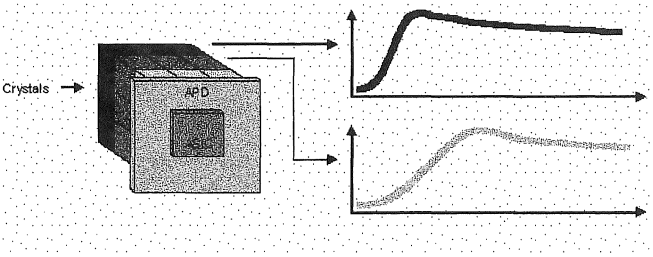

Fig. 2 A detector module for PSD. DOI information can be obtained from the different rise times of the preamplifier as shown.

II. First WSFE chip design and results

A first generation 8-ch WSFE chip has been designed and experimental results of each component are given below.

1. Charge Sensitive Preamplifier (CSA)

(1) Design of Preamplifier

The traditional architecture—cascode topology, has been implemented in this chip. Here a regulated cascode topology[3)] is adopted by adding a local feedback loop to control the gate voltage of the cascode transistor. The schematic of the CSA is shown in **Fig.3**. M1 is the input transistor and the local feedback by the transistor Mreg enlarges the difference

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between the dominant pole at the drain of M2 (b in **Fig.3**) and the non-dominant pole at the drain of M1 (a in **Fig.3**), which enables frequency compensation.

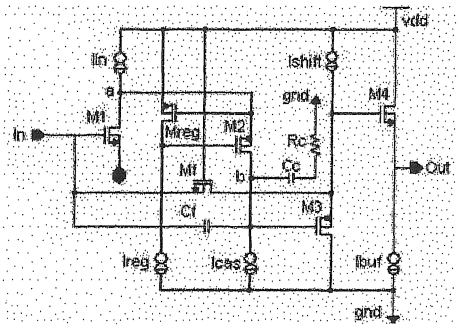

Fig.3 Schematic of the preamplifier

(2) Test results of the preamplifier

A fast rise time of about 10ns is necessary to accurately obtain timing information and carry out PSD. Besides, low noise is also required as the gains of APDs are much lower than PMTs, implying a lower signal to noise ratio. However, the rise time of the preamplifier is 22 ns and the optimum Equivalent Noise Count (ENC) is about 4600 e- fwhm (or 1960 e- r.m.s) at shaping time of 6 μs, which is quite high and not suitable for our application where a shorter shaping time is desired (see **Fig. 4**)

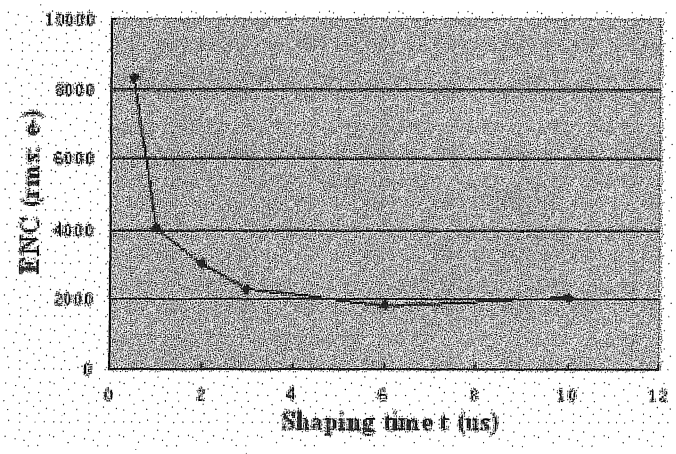

Fig. 4 Noise characteristic of the preamplifier

The main reason for slow rise time is the poor driving ability of the preamplifier. An unnecessary heavy load was introduced while inspecting intermediate loads. However, this loading effect should not be significant when driving on-chip devices. The high ENC is probably due to poor layout of the preamplifier. Parasitic coupling between components of close proximity can give rise to unwanted currents and capacitances which lead to slight oscillation in the output signal. Thin interconnecting wires may also introduce serial resistance between the input transistor and voltage supply, which will in turn degrade the speed and noise performance of the preamplifier.

2. Variable Gain Amplifier

(1) Design of the VGA

The VGA is based on the Norton amplifier[4] and the schematic is shown in **Fig.5**. The gain was designed to vary from 5 to 40.

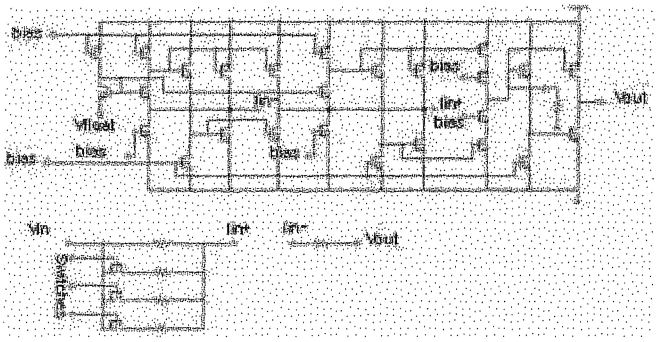

Fig. 5 Schematic of the VGA

(2) Test results of the VGA

Test of the chip showed that the actual gain can be varied from 3.6 up to a value of about 25 and the reason for the lower gain is probably because the input resistance of the Norton amplifier is not low enough. The rise time of the VGA is about 20~30ns.

3. 6-bit Folding ADC

(1) Principle and design of the folding ADC

A 6-bit 100 MSPS folding ADC was designed to accurately sample the output of preamplifier[5]. The folding ADC is a modified version of the Flash ADC but with folders to reduce the number of comparators needed and hence the power consumption while not losing its advantage of high speed and low latency. The working principle of the folding ADC is explained in **Fig. 6**. The most significant bits of the input signal is identified by sensing which segment of the folds it lays while the least significant bits are obtained as with a flash ADC. The nonlinearity of the folder in the realistic case can be overcome by using multiple folders.

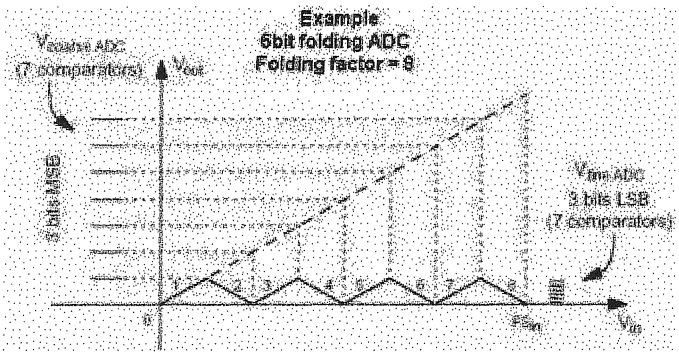

Fig. 6 An example of an ideal 6-bit folding ADC

The schematic of a folder used in our design is shown in **Fig. 7**. We used 8 folders (folding factor of 4) and 18 comparators, 2 for each folder and 2 to obtain the most significant bit (MSB).

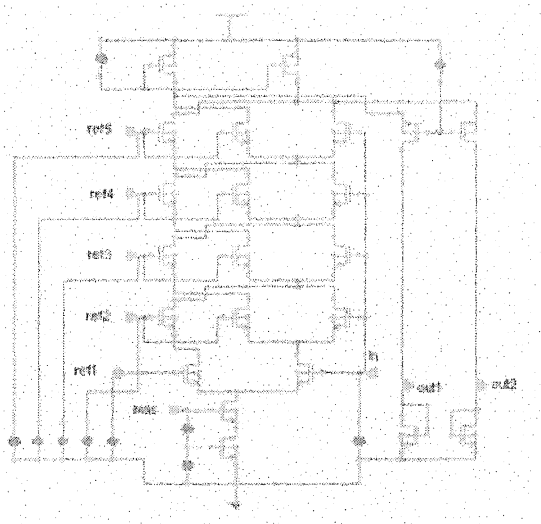

Fig. 7 Schematic of the folding amp

(2) Test results of the folding ADC

This folding ADC is linear (see **fig. 8**) and functions well at least up to a sampling rate of 50 MHz. The power consumption for 8 channels is approximately 1.2 W at that rate. A faster rise time is required to achieve faster sampling rate.

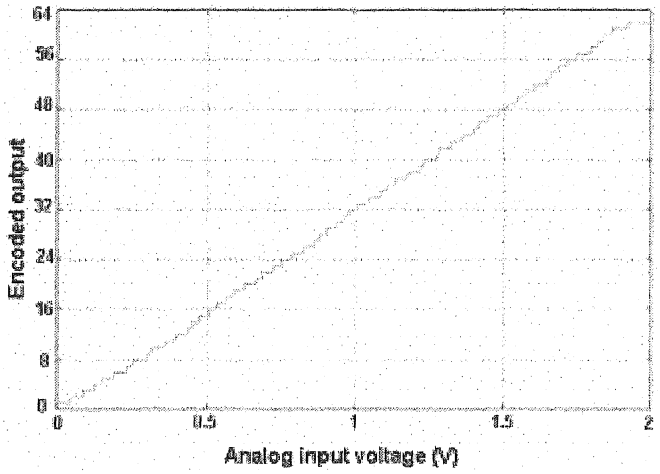

Fig.8 Transfer function of the Folding ADC

The differential nonlinearity (DNL) is 0.7 LSB while the integral nonlinearity (INL) is 1.4 LSB. The Total Harmonic Distortion (THD), albeit not a critical factor in our application, is -20 dB.

III. Improved WSFE chip design and results

Since the results from the first chip were not as expected, a new 10-ch chip was designed and test results are presented in this section. The micrograph of this chip is shown in **Fig. 9**.

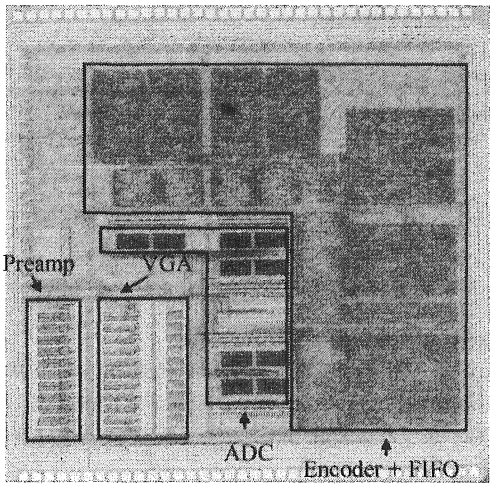

Fig. 9 Layout of the new 10-ch WSFE ASIC

1. Results of the new Charge Sensitive Preamplifier (CSA)

The rise time of the preamplifier is about 25 ns and the optimum Equivalent Noise Count (ENC) is 1300 e- fwhm at shaping time of 0.5 μs as shown is **Fig. 10**. This value is an improvement of several folds over the previous chip at the expense of a smaller output swing as telescopic-cascode structure was implemented and is evident in **Fig. 11**. A rise time of less than 25ns was expected from the high cascode stage gain.

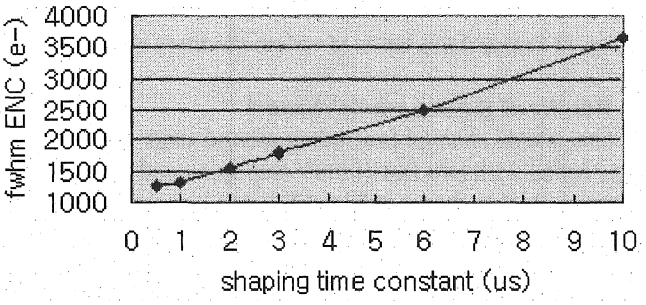

Fig. 10 Noise characteristic of preamp

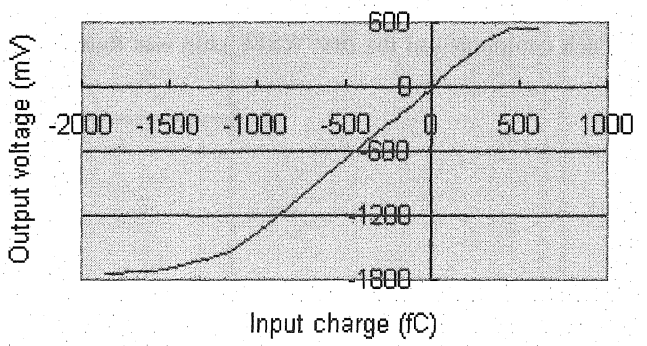

Fig. 11 Linearity of the preamp

2. Results of the new Variable Gain Amplifier (VGA)

A two stage VGA was designed. The rise time of the first stage is about 20ns and the gain can be varied from about 3.6 to 12.7 as given in **table 1**. However, the second stage was not

not working as desired.

Table 1 First stage gain of the VGA

VGA gain control input	*Gain*
00	3.6
01	6.9
10	10.0
11	12.7

3. Results of the new Folding ADC

The new folding ADC works at least up to a rate of 100 MHz. Sampled step input of various rise times are shown in **Fig. 12**. The DNL and INL were calculated to be 1.1 LSB and 1.4 LSB respectively.

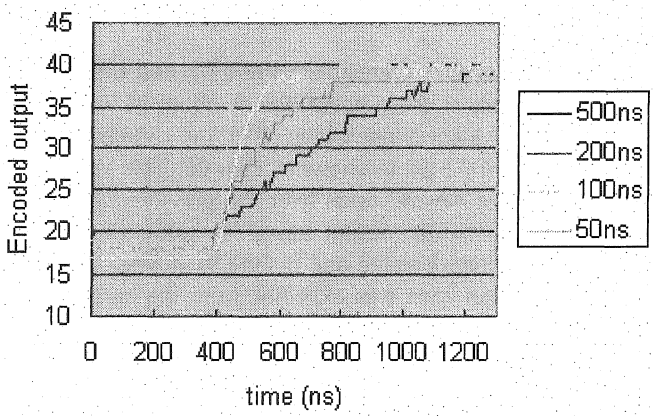

Fig. 12 Sampled step inputs of various rise times with the ADC

4. Results of the one whole channel

One whole channel (excluding second stage of the VGA) was tested with two fast 100mV step input and the digitized output signal is shown in **Fig. 13**. It can be seen that the two signals can be distinguished from one another although not very distinct. The power consumption is about 1.2W for the whole chip.

IV. Conclusions

Each component of the first WSFE chip was found to be working although not as designed. Most of the observed inconsistencies between simulation results and measured results arise from the inaccuracy of our simulation related to the layout process and the fabrication process parameters. Careful considerations of the layouts and testability of the chip produced a significantly improved second chip although more modifications seem inevitable.

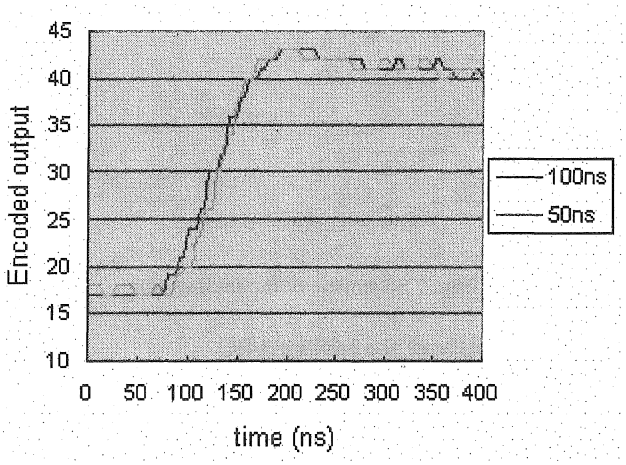

Fig. 13 Sampled step inputs using whole channel

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